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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/23/2004 17

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,615	YIM ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the multiplexer transmitting one of the column cycle signal and the read control signal to the gate of the second transistor in response to a clock enable signal of Claim 4 must be shown or the feature(s) canceled from the claim(s). Figure 4 shows the multiplexer transmitting a signal to the calibration controller, which then transmits the signal to the gate of the second transistor. Figure 4 does not show the multiplexer connected directly to the gate of the second transistor. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 11 is objected to because of the following informalities: On Line 3, the word "an" appears to have been erroneously inserted in place of the word "and"; On Line 4, the word "to" appears to have been erroneously inserted between the words "data" and "through". Appropriate correction is required.

4. Claim 12 is objected to because of the following informalities: In the original application filed 27 December 2000, Claim 12 is a dependent claim of independent claim 13. In the amendment filed 23 December 2003, Claim 12, while being designated as "original", is a dependent claim of independent claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 7 recites the limitation "the data input/output lines" in Line 5. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 10 recites the limitation "the data input/output line" in Lines 1-3. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 15 recites the limitation "the characteristics of the data input/output line" in Lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 3, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art ("AAPA"), US Patent Number 4,745,407 to Costello ("Costello"), and US Patent Number 5,915,105 to Farmwald et al. ("Farmwald").

11. In reference to Claim 1, AAPA teaches an output driver in a semiconductor memory device including a plurality of blocks of memory cells (See Figure 1 and Page 1 Lines 36-37); wherein a first of the blocks transmits data to a data input/output line through the output driver (See Figures 1 and 2 and Page 1 Lines 36-37, and Page 2 Lines 14-23); the output driver comprising a first transistor connected to a reference voltage and the first transistor being responsive to the data from the first block (See Figure 2 Number MN2 and Page 2 Lines 20-21); a second transistor between the first

transistor and the data input/output line (See Figure 2 Number MN1); and a controller coupled to control the second transistor (See Figure 1 Number 10 and Page 2 Lines 16-20). AAPA does not teach that the controller includes a multiplexer; the controller being operable in a first mode in which the second transistor is responsive to a read control signal and a column cycle signal for selecting the first block; and wherein the data from the first block is transmitted to the data input/output line via the first and second transistors. Costello teaches a memory device that transfers data from a block when it responds to a read signal and a column signal (See Column 11 Lines 26-35). Farmwald teaches output drivers being controlled by a multiplexer with two or more inputs connected to other internal chip circuitry (See Figure 10 and Column 22 Lines 7-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello and the multiplexer controlled output driver of Farmwald, resulting in the invention of Claim 1, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39 of Costello) and because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald).

12. In reference to Claim 3, AAPA, Costello, and Farmwald teach the limits as applied to Claim 1 above. AAPA further teaches the controller activating the second transistor by sending a VgateN signal, which is analogous to a read control signal (See Figure 2 and Page 2 Lines 16-20 and 24-26); and when the second transistor responds

to the VgateN signal, the data from the first block is transmitted to the data input/output line via the first and second transistors (See Figure 2 and Page 2 Lines 14-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello and the multiplexer controlled output driver of Farmwald, resulting in the invention of Claim 3, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39 of Costello) and because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald).

13. In reference to Claim 11, AAPA teaches a semiconductor memory device comprising a plurality of output drivers (See Figures 1 and 2 and Page 2 Lines 14-15); a plurality of blocks of memory cells corresponding to and respectively coupled to the plurality of output drivers, wherein each block transmits data through the corresponding output driver (See Figures 1 and 2, Page 1 Lines 36-37, and Page 2 Lines 14-23); wherein a first of the blocks transmits data to a data input/output line through the output driver (See Figures 1 and 2 and Page 2 Lines 14-23); each output driver comprising a first transistor connected to a reference voltage and the first transistor being responsive to the data from the corresponding block (See Figure 2 Number MN2 and Page 2 Lines 20-21); a second transistor connected to the first transistor (See Figure 2 Number MN1); a controller coupled to control the second transistor (See Figure 1 Number 10 and Page 2 Lines 16-20); and the controller operable in a mode in which the second

transistor is responsive to a VgateN signal, which is analogous to a read control signal (See Figure 2 and Page 2 Lines 16-20 and 24-26). AAPA does not teach that the controller includes a multiplexer; the controller being operable in a first mode in which the second transistor is responsive to a read control signal and a column cycle signal for selecting the block corresponding to the output driver. Costello teaches a memory device that transfers data from a block when it responds to a read signal and a column signal (See Column 11 Lines 26-35). Farmwald teaches output drivers being controlled by a multiplexer with two or more inputs connected to other internal chip circuitry (See Figure 10 and Column 22 Lines 7-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello and the multiplexer controlled output driver of Farmwald, resulting in the invention of Claim 11, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39 of Costello) and because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald).

14. In reference to Claim 14, AAPA, Costello, and Farmwald teach the limits as applied to Claim 11 above. Costello teaches a memory device that transfers data from a block when it responds to a read signal and a column signal (See Column 11 Lines 26-35). Farmwald teaches output drivers being controlled by a multiplexer controlled by a clock signal with two or more inputs connected to other internal chip circuitry, such as

the read signal and column signal of Costello (See Figure 10 and Column 22 Lines 7-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello and the multiplexer controlled output driver of Farmwald, resulting in the invention of Claim 14, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39 of Costello) and because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald).

15. Claims 2, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Costello, and Farmwald as applied to Claims 1 and 11 above, and further in view of US Patent Number 6,266,252 to Karabatsos ("Karabatsos").

16. In reference to Claim 2, AAPA, Costello, and Farmwald teach the limitations as applied to Claim 1 above. AAPA, Costello, and Farmwald do not teach that the controller deactivates the second transistor when a second of the blocks is selected for data output. Karabatsos teaches connecting each memory element to a FET switch and turning the FET switch on to connect a selected memory element to a bus while keeping non-selected memory elements isolated from the bus by keeping their associated FET switches off (See Figure 1, Column 4 Lines 29-42, and Column 5 Lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the selective memory device activation of Karabatsos, resulting in the invention of Claim 2, in order to negate the additive effects of line capacitance (See Column 2 Lines 65-67 and Column 3 Lines 1-2 of Karabatsos), increase speed (See Column 2 Lines 51-64 of Karabatsos), and enhance memory speed and capacity (See Abstract of Karabatsos).

17. In reference to Claim 12, AAPA, Costello, and Farmwald teach the limitations as applied to Claim 1 above. AAPA, Costello, and Farmwald do not teach that the controllers deactivate the second transistors of the output drivers in unselected blocks. Karabatsos teaches connecting each memory element to a FET switch and turning the FET switch on to connect a selected memory element to a bus while keeping non-selected memory elements isolated from the bus by keeping their associated FET switches off (See Figure 1, Column 4 Lines 29-42, and Column 5 Lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the selective memory device activation of Karabatsos, resulting in the invention of Claim 12, in order to negate the additive effects of line capacitance (See Column 2 Lines 65-67 and Column 3 Lines 1-2 of Karabatsos), increase speed (See Column 2 Lines 51-64 of Karabatsos), and enhance memory speed and capacity (See Abstract of Karabatsos).

18. In reference to Claim 12, AAPA, Costello, and Farmwald teach that the limitations as applied to Claim 11 above. AAPA, Costello, and Farmwald do not teach the controllers deactivate the second transistors of the output drivers in unselected blocks. Karabatsos teaches connecting each memory element to a FET switch and turning the FET switch on to connect a selected memory element to a bus while keeping non-selected memory elements isolated from the bus by keeping their associated FET switches off (See Figure 1, Column 4 Lines 29-42, and Column 5 Lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the selective memory device activation of Karabatsos, resulting in the invention of Claim 12, in order to negate the additive effects of line capacitance (See Column 2 Lines 65-67 and Column 3 Lines 1-2 of Karabatsos), increase speed (See Column 2 Lines 51-64 of Karabatsos), and enhance memory speed and capacity (See Abstract of Karabatsos).

19. In reference to Claim 13, AAOA, Costello, and Farmwald teach the limitations as applied to Claim 11 above. AAPA further teaches that the output driver enable signals are simultaneously provided to the second transistors to activate said second transistors simultaneously during the second mode (See Figure 2 and Page 2 Lines 24-26). AAPA, Costello, and Farmwald do not teach that the controller signal separately activates the associated second transistor of the output driver during the first mode. Karabatsos

teaches connecting each memory element to a FET switch and turning the FET switch on to connect a selected memory element to a bus while keeping non-selected memory elements isolated from the bus by keeping their associated FET switches off (See Figure 1, Column 4 Lines 29-42, and Column 5 Lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the selective memory device activation of Karabatsos, resulting in the invention of Claim 12, in order to negate the additive effects of line capacitance (See Column 2 Lines 65-67 and Column 3 Lines 1-2 of Karabatsos), increase speed (See Column 2 Lines 51-64 of Karabatsos), and enhance memory speed and capacity (See Abstract of Karabatsos).

20. Claims 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Costello, and Farmwald as applied to Claim 1 above, and further in view of US Patent Number 6,513,103 to Garlepp et al. ("Garlepp").

21. In reference to Claim 4, AAPA, Costello, and Farmwald teach the limitations as in Claim 1 above. AAPA, Costello, and Farmwald do not teach that the controller is further operable in a second mode in which the second transistor is responsive to a read control signal containing calibration information about characteristics of the data input/output line. AAPA further teaches the second transistor being responsive to a VgateN signal, which is analogous to a read control signal (See Figure 2 and Page 2

Lines 16-20 and 24-26). Garlepp teaches detecting information about the system such as frequency, voltage, and temperature (analogous to calibration information) and providing that information to memory devices connected to the system in order to tune their performance (See Column 3 Lines 47-61 and Column 4 Lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the providing of calibration information to attached memory devices of Garlepp, resulting in the invention of Claim 4, in order to allow the system to tune the performance of it's memory interface (See Column 3 Lines 65-67 and Column 4 Lines 1-5 of Garlepp) and because detecting and storing this type of information is known in the art (See Column 3 Lines 62-64 of Garlepp).

22. In reference to Claim 5, AAPA, Costello, Farmwald, and Garlepp teach the limits as applied to Claim 4 above. Costello teaches a memory device that transfers data from a block when it responds to a read signal and a column signal (See Column 11 Lines 26-35). Farmwald teaches output drivers being controlled by a multiplexer controlled by a clock signal with two or more inputs connected to other internal chip circuitry, such as the read signal and column signal of Costello (See Figure 10 and Column 22 Lines 7-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the providing of calibration information to attached memory devices of Garlepp,

resulting in the invention of Claim 5, in order to allow the system to tune the performance of it's memory interface (See Column 3 Lines 65-67 and Column 4 Lines 1-5 of Garlepp) and because detecting and storing this type of information is known in the art (See Column 3 Lines 62-64 of Garlepp).

23. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Costello, Farmwald, and Garlepp as applied to Claim 4 above, and further in view of US Patent Number 5,959,481 to Donnelly et al. ("Donnelly") and US Patent Number 6,417,653 to Massie et al. ("Massie").

24. In reference to Claim 6, AAPA, Costello, Farmwald, and Garlepp teach the limits as applied to Claim 4 above. AAPA, Costello, Farmwald, and Garlepp do not teach the characteristics of the data input/output line comprising an output current characteristic for adjusting a signal level of the data input/output line and a temperature characteristic for adjusting a slew rate of the output driver according to change in temperature. Garlepp further teaches that the information about the system includes information that affects circuit functioning, such as temperature (See Column 3 Lines 51-55). An output current characteristic would inherently be information that affects circuit functioning. Donnelly teaches a bus driving circuit that adjusts the slew rate in response to temperature (See Column 3 Lines 51-58). Massie teaches a circuit that adjusts the output voltage signal level as a function of the output current (See Column 2 Lines 49-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, Farmwald, and Garlepp with the temperature controlled slew rate of Donnelly and the output current controlled output signal of Massie, resulting in the invention of Claim 6, in order to compensate for slew rate variations as they occur and thus reduce the range of values across which the slew rate may vary (See Column 3 Lines 64-67 of Donnelly); and to provide an increased voltage margin to respond to load changes producing output current signal changes (See Column 2 Lines 55-58 of Massie).

25. Claims 7, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Costello, Farmwald, and Garlepp.

26. In reference to Claim 7, AAPA teaches a plurality of semiconductor memory devices (See Figures 1 and 2); a plurality of blocks of memory cells (See Figures 1 and 2); a plurality of output drivers corresponding to the blocks the blocks transmitting data through output drivers (See Figures 1 and 2); channel bus lines shared by the data input/output lines (See Figures 1, 2, and 3, and Page 2 Lines 6-7 which was amended on 10 September 2003); the data of a selected block is transmitted to one of the channel bus lines via a corresponding output driver (See Figure 2); and via one of the data input/output line (See Figures 1, 2, and 3); the output driver comprising a first transistor connected to a reference voltage and responsive to the memory cell data (See Figure 2). AAPA does not teach that the output driver is activated in response to a

column cycle signal selecting the block; the output drivers all being deactivated in the remaining semiconductor memory devices sharing the channel bus line; and a second transistor for selectively connecting the first transistor to the data input/output line in response to the column cycle signal or a read control signal containing calibration information about characteristics of the data input/output line. Costello teaches a memory device that transfers data from a block when it responds to a read signal and a column signal (See Column 11 Lines 26-35). Because the memory device inherently has an output driver and the memory device transfers data from a block when it responds to a read signal and a column signal, the output driver for the block must inherently be activated in response to said column signal. Farmwald teaches output drivers being controlled by a multiplexer with two or more inputs connected to other internal chip circuitry (See Figure 10 and Column 22 Lines 7-26). Garlepp teaches detecting information about the system such as frequency, voltage, and temperature (analogous to calibration information) and providing that information to memory devices connected to the system in order to tune their performance (See Column 3 Lines 47-61 and Column 4 Lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello, the multiplexer controlled output driver of Farmwald, and the providing of calibration information to attached memory devices of Garlepp, resulting in the invention of Claim 7, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39

of Costello); because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald); to allow the system to tune the performance of it's memory interface (See Column 3 Lines 65-67 and Column 4 Lines 1-5 of Garlepp); and because detecting and storing this type of information is known in the art (See Column 3 Lines 62-64 of Garlepp).

27. In reference to Claim 8, AAPA, Costello, Farmwald, and Garlepp teach the limits as applied to Claim 7 above. AAPA further teaches that the output driver enable signals (analogous to the read control signals) are simultaneously provided to the second transistors to activate said second transistors simultaneously (See Figure 2 and Page 2 Lines 24-26); and transmitting the memory cell data of the selected block to the data input/output line via the first and second transistors (See Figure 2 and Page 2 Lines 16-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello, the multiplexer controlled output driver of Farmwald, and the providing of calibration information to attached memory devices of Garlepp, resulting in the invention of Claim 8, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39 of Costello); because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald); to allow the system to tune the performance of it's memory interface (See Column 3 Lines 65-67 and Column 4

Lines 1-5 of Garlepp); and because detecting and storing this type of information is known in the art (See Column 3 Lines 62-64 of Garlepp).

28. In reference to Claim 9, AAPA, Costello, Farmwald, and Garlepp teach the limits as applied to Claim 7 above. Costello teaches a memory device that transfers data from a block when it responds to a read signal and a column signal (See Column 11 Lines 26-35). Farmwald teaches output drivers being controlled by a multiplexer controlled by a clock signal with two or more inputs connected to other internal chip circuitry, such as the read signal and column signal of Costello (See Figure 10 and Column 22 Lines 7-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory device of AAPA with the response to a read signal and a column signal of Costello, the multiplexer controlled output driver of Farmwald, and the providing of calibration information to attached memory devices of Garlepp, resulting in the invention of Claim 9, in order to allow two eight bit bytes to be transferred onto the bus in one operation (See Column 11 Lines 22-25 and Lines 37-39 of Costello); because memory devices with multiplexer controlled output drivers are well known in the art (See Column 22 Lines 22-26 of Farmwald); to allow the system to tune the performance of it's memory interface (See Column 3 Lines 65-67 and Column 4 Lines 1-5 of Garlepp); and because detecting and storing this type of information is known in the art (See Column 3 Lines 62-64 of Garlepp).

29. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Costello, Farmwald, and Garlepp as applied to Claim 7 above, and further in view of Donnelly, and Massie.

30. In reference to Claim 10, AAPA, Costello, Farmwald, and Garlepp teach the limits as applied to Claim 7 above. AAPA, Costello, Farmwald, and Garlepp do not teach the characteristics of the data input/output line being an output current characteristic of adjusting the signal level of the data input/output line and a temperature characteristic of adjusting the slew rate of the output driver according to change in temperature. Garlepp further teaches that the information about the system includes information that affects circuit functioning, such as temperature (See Column 3 Lines 51-55). An output current characteristic would inherently be information that affects circuit functioning. Donnelly teaches a bus driving circuit that adjusts the slew rate in response to temperature (See Column 3 Lines 51-58). Massie teaches a circuit that adjusts the output voltage signal level as a function of the output current (See Column 2 Lines 49-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, Farmwald, and Garlepp with the temperature controlled slew rate of Donnelly and the output current controlled output signal of Massie, resulting in the invention of Claim 10, in order to compensate for slew rate variations as they occur and thus reduce the range of values across which the slew rate may vary (See Column 3 Lines 64-67 of Donnelly); and to

provide an increased voltage margin to respond to load changes producing output current signal changes (See Column 2 Lines 55-58 of Massie).

31. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Costello, and Farmwald as applied to Claim 11 above, and further in view of Garlepp, Donnelly, and Massie.

32. In reference to Claim 15, AAPA, Costello, and Farmwald teach the limitations as applied to Claim 11 above. AAPA, Costello, and Farmwald do not teach that the characteristics of the data input/output line comprise and output current characteristic for adjusting a signal level of the data input/output line and a temperature characteristic for adjusting a slew rate of the output driver according to a change in temperature. Garlepp teaches detecting information about the system such as frequency, voltage, and temperature (analogous to calibration information) and providing that information to memory devices connected to the system in order to tune their performance (See Column 3 Lines 47-61 and Column 4 Lines 1-5). Garlepp further teaches that the information about the system includes information that affects circuit functioning, such as temperature (See Column 3 Lines 51-55). An output current characteristic would inherently be information that affects circuit functioning. Donnelly teaches a bus driving circuit that adjusts the slew rate in response to temperature (See Column 3 Lines 51-58). Massie teaches a circuit that adjusts the output voltage signal level as a function of the output current (See Column 2 Lines 49-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the memory system of AAPA, Costello, and Farmwald with the providing of calibration information to attached memory devices of Garlepp, the temperature controlled slew rate of Donnelly, and the output current controlled output signal of Massie resulting in the invention of Claim 15, in order to allow the system to tune the performance of it's memory interface (See Column 3 Lines 65-67 and Column 4 Lines 1-5 of Garlepp); because detecting and storing this type of information is known in the art (See Column 3 Lines 62-64 of Garlepp); order to compensate for slew rate variations as they occur and thus reduce the range of values across which the slew rate may vary (See Column 3 Lines 64-67 of Donnelly); and to provide an increased voltage margin to respond to load changes producing output current signal changes (See Column 2 Lines 55-58 of Massie).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4:30), Alt. Fridays (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

tjc

Thomas J. Cleary
Patent Examiner
Art Unit 2111